

IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of the claims in the application:

1.(Original) A method for forming a modified semiconductor having a plurality of band gaps, the method comprising the steps of:

providing a semiconductor having a surface and a quantum region which emits photons in response to electrical or optical stimulation, the quantum region having an original band gap and being disposed under said surface;

applying a plurality of layers of a plurality of materials to a plurality of selected regions of said surface, said plurality of materials being adapted to cause, upon thermal annealing, a plurality of degrees of intermixing in a plurality of portions of said quantum region disposed immediately below each of said selected regions of said surface; and

thermally annealing said plurality of layers to said surface such that said layers of said materials cause said plurality of degrees of intermixing in said plurality of portions of said quantum region thereby shifting the original band gaps of said portions of said quantum region,

thereby forming a modified semiconductor which exhibits a plurality of different band gaps in said plurality of portions of said quantum region depending upon the positioning of said plurality of layers of said plurality of materials on the surface immediately above the respective portions of said quantum region.

2.(Original) A method according to claim 1 wherein said plurality of layers comprises between two and five layers and wherein said plurality of materials comprises between two and five materials.

3.(Currently amended) A method according to claim 1 wherein at least one of said materials is selected from the group ~~comprising~~ consisting of:

(a) SiO₂; ~~or~~ and

- (b) Si_xN_y , wherein x and y are integers greater than 0.

4.(Original) A method according to claim 3 wherein said step of applying said plurality of layers of said plurality of materials to said plurality of selected regions of said surface comprises applying at least one of layers using one or more of the following techniques:

- (a) plasma enhanced chemical vapor deposition (PECVD);
- (b) E-beam evaporation; or
- (c) the spin-on method.

5.(Currently amended) A method according to claim 1 wherein at least one of said materials is selected from the group ~~comprising~~ consisting of:

- (a) LTInP (low temperature deposited InP); ~~or~~ and
- (b) LT(In)GaAs (low temperature deposited InGaAs or GaAs).

6.(Original) A method according to claim 5 wherein said step of applying said plurality of layers of said plurality of materials to said plurality of selected regions of said surface comprises applying at least one of said layers using one or more of the following techniques at a lower epitaxy temperature:

- (a) metal organic chemical vapor deposition (MOCVD); or
- (b) molecular beam epitaxy (MBE).

7.(Previously presented) A method according to claim 1 wherein the step of applying a plurality of layers of a plurality of materials to a plurality of selected regions of said surface comprises applying one or more of said layers in a pattern.

8.(Original) A method according to claim 7 wherein said step of applying one or more of said layers in a pattern comprises:

- (a) applying said layer to said selected region of said surface; and

- (b) patterning said layer using one or more of the following techniques:
 - (i) photolithography; or
 - (ii) electron-beam lithography.

9.(Currently amended) A method according to claim 7 wherein said step of applying one or more of said layers in a pattern comprises applying said one or more layers in one or more modes selected from the group ~~comprising~~ consisting of:

- (a) a dot pattern comprising a plurality of dots separated by a plurality of spaces;
- (b) an inverse dot pattern comprising a plurality of inverse dots separated by a plurality of inverse spaces;
- (c) a line pattern comprising a plurality of lines separated by a plurality of spaces;
- (d) an inverse line pattern comprising a plurality of inverse lines separated by a plurality of inverse spaces; ~~or~~ and
- (e) a planar pattern.

10.(Original) A method according to claim 9 wherein said dots, inverse dots, lines and inverse lines have relatively uniform diameters within each pattern and wherein said spaces and inverse spaces are relatively uniform within each pattern.

11.(Original) A method according to claim 10 wherein said diameters of said dots are less than or equal to 2 μm .

12.(Previously presented) A method according to claim 10 wherein said spaces and inverse spaces are less than or equal to 2 μm .

13.(Previously presented) A method according to claim 1 wherein said step of applying said plurality of layers of said plurality of materials to said plurality of selected regions of said surface comprises applying said layers to a thickness ranging from 10 nm to 500 nm.

14.(Previously presented) A method according to claim 1 wherein said step of thermally annealing said heterostructure comprises rapidly thermally annealing said heterostructure by heating said heterostructure at temperatures ranging from 500 to 1000° C for periods of time ranging from 1 to 1000 seconds.

15.(Previously presented) A method according to claim 1 wherein said semiconductor comprises:

- (a) a semiconductor substrate; and
- (b) a quantum region.

16.(Original) A method according to claim 15 wherein said semiconductor substrate is made from either:

- (a) InP; or
- (b) GaAs.

17.(Previously presented) A method according to claim 15 wherein said quantum region comprises one or more of:

- (a) a single quantum well structure;
- (b) a multiple quantum well structure;
- (c) a super lattice structure;
- (d) a quantum wire structure; or
- (e) a quantum dot structure.

18.(Original) A method according to claim 17 wherein said quantum well structure comprises of one or more of:

- (a) InGaAsP/InGaAsP;

- (b) InGaAsP/InP;
- (c) InGaAs/InP;
- (d) GaAs/AlGaAs;
- (e) InGaAs/GaAs;
- (f) InGaAlAs/GaAs; or
- (g) InGaAsN/GaAs.

19.(Canceled)

20.(Canceled)

21.(Original) A modified semiconductor having a plurality of band gaps, the semiconductor comprising:

- (a) a surface;
- (b) a quantum region which emits photons in response to electrical or optical stimulation, the quantum region having an original band gap and being disposed under said surface; and
- (c) a plurality of layers of a plurality of materials disposed on a plurality of selected regions of said surface, said plurality of materials being adapted to cause, upon thermal annealing, a plurality of degrees of intermixing in a plurality of portions of said quantum region disposed immediately below each of said selected regions of said surface;

wherein the plurality of layers are thermally annealed to said surface,

and wherein said modified semiconductor exhibits a plurality of different band gaps in said plurality of portions of said quantum region according to the positioning of said plurality of layers of said plurality of materials on the surface immediately above the respective portions of said quantum region.

Claim 22 (Cancelled)

23.(Currently amended) A method according to claim 2 wherein at least one of said

materials is selected from the group ~~comprising~~ consisting of:

- (a) SiO_2 ; ~~or~~ and
- (b) Si_xN_y , wherein x and y are integers greater than 0.

24.(Previously presented) A method according to claim 23 wherein said step of applying said plurality of layers of said plurality of materials to said plurality of selected regions of said surface comprises applying at least one of layers using one or more of the following techniques:

- (a) plasma enhanced chemical vapor deposition (PECVD);
- (b) E-beam evaporation; or
- (c) the spin-on method.

25.(Currently amended) A method according to claim 2 wherein at least one of said materials is selected from the group ~~comprising~~ consisting of:

- (a) LTInP (low temperature deposited InP); ~~or~~ and
- (b) LT(In)GaAs (low temperature deposited InGaAs or GaAs).

26.(Previously presented) A method according to claim 25 wherein said step of applying said plurality of layers of said plurality of materials to said plurality of selected regions of said surface comprises applying at least one of said layers using one or more of the following techniques at a lower epitaxy temperature:

- (a) metal organic chemical vapor deposition (MOCVD); or
- (b) molecular beam epitaxy (MBE).

27.(Previously presented) A method according to claim 2 wherein the step of applying a plurality of layers of a plurality of materials to a plurality of selected regions of said surface comprises applying one or more of said layers in a pattern.

28.(Currently amended) A method according to claim 27 wherein at least one of said

materials is selected from the group ~~comprising~~ consisting of:

- (a) SiO_2 ; ~~or~~ and
- (b) Si_xN_y , wherein x and y are integers greater than 0.

29.(Previously presented) A method according to claim 28 wherein said step of applying said plurality of layers of said plurality of materials to said plurality of selected regions of said surface comprises applying at least one of layers using one or more of the following techniques:

- (a) plasma enhanced chemical vapor deposition (PECVD);
- (b) E-beam evaporation; or
- (c) the spin-on method.

30.(Currently amended) A method according to claim 29 wherein at least one of said materials is selected from the group ~~comprising~~ consisting of:

- (a) LTInP (low temperature deposited InP); ~~or~~ and
- (b) LT(In)GaAs (low temperature deposited InGaAs or GaAs).

31.(Previously presented) A method according to claim 30 wherein said step of applying said plurality of layers of said plurality of materials to said plurality of selected regions of said surface comprises applying at least one of said layers using one or more of the following techniques at a lower epitaxy temperature:

- (a) metal organic chemical vapor deposition (MOCVD); or
- (b) molecular beam epitaxy (MBE).

32.(Previously presented) A method according to claim 27 wherein said step of applying one or more of said layers in a pattern comprises:

- (a) applying said layer to said selected region of said surface; and
- (b) patterning said layer using one or more of the following techniques:
 - (i) photolithography; or

- (ii) electron-beam lithography.

33.(Previously presented) A method according to claim 32 wherein said step of applying one or more of said layers in a pattern comprises applying said one or more layers in one or more of:

- (a) a dot pattern comprising a plurality of dots separated by a plurality of spaces;
- (b) an inverse dot pattern comprising a plurality of inverse dots separated by a plurality of inverse spaces;
- (c) a line pattern comprising a plurality of lines separated by a plurality of spaces;
- (d) an inverse line pattern comprising a plurality of inverse lines separated by a plurality of inverse spaces; or
- (e) a planar pattern.

34.(Previously presented) A method according to claim 33 wherein said dots, inverse dots, lines and inverse lines have relatively uniform diameters within each pattern and wherein said spaces and inverse spaces are relatively uniform within each pattern.

35.(Previously presented) A method according to claim 34 wherein said diameters of said dots and lines is less than or equal to 2 μm .

36.(Previously presented) A method according to claim 35 wherein said spaces and inverse spaces are less than or equal to 2 μm .

37.(Previously presented) A method according to claim 23 wherein said step of applying said plurality of layers of said plurality of materials to said plurality of selected regions of said surface comprises applying said layers to a thickness ranging from 10 nm to 500 nm.

38.(Previously presented) A method according to claim 27 wherein said step of applying

said plurality of layers of said plurality of materials to said plurality of selected regions of said surface comprises applying said layers to a thickness ranging from 10 nm to 500 nm.

39.(Previously presented) A method according to claim 27 wherein said step of thermally annealing said heterostructure comprises rapidly thermally annealing said heterostructure by heating said heterostructure at temperatures ranging from 500 to 1000° C for periods of time ranging from 1 to 1000 seconds.

40.(Previously presented) A method according to claim 27 wherein said semiconductor comprises:

- (a) a semiconductor substrate; and
- (b) a quantum region.

41.(Previously presented) A method according to claim 40 wherein said semiconductor substrate is made from either:

- (a) InP; or
- (b) GaAs.

42.(Previously presented) A method according to claim 41 wherein said quantum region comprises one or more of:

- (a) a single quantum well structure;
- (b) a multiple quantum well structure;
- (c) a super lattice structure;
- (d) a quantum wire structure; or
- (e) a quantum dot structure.

43.(Previously presented) A method according to claim 42 wherein said quantum well

structure comprises of one or more of:

- (a) InGaAsP/InGaAsP;
- (b) InGaAsP/InP;
- (c) InGaAs/InP;
- (d) GaAs/AlGaAs;
- (e) InGaAs/GaAs;
- (f) InGaAlAs/GaAs; or
- (g) InGaAsN/GaAs.

Claim 44 (Cancelled)